Condor Internal Software Protocol

Note that this document does not include software related to interface with the MIU (customer computer) or software related to internal determination of the FPGA (e.g. memory usage, ETM, etc.). This document only includes software related to communication between PSU system components and to any calculations required by the FPGA related to reporting measurements or status bits.

## Background

The Condor PSU produces 10 outputs according to Table I. The PSU consists of system components and controllers which are summarized in Table II.

**TABLE I – Inputs and Outputs**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **INPUT** | **output**  **#** | **Output**  **Voltage** | **OUTPUT POWER** | | | **Hold-Up Time (ms)** | **Target ELOP System** |
| Typical Continuous | Maximum Continuous | Transient/Peak |
| **28VDC** | 1 | 36VDC | 150W | 220W | 250W (<5s) | 0 | FAN CCA |
| **115VAC**  **3Ø 400Hz** | 2 | 30.5VDC | 20W | 50W | 150W (<50ms) | 10 | MWIR  COOLER |
| 3 | 115VAC  3Ø | 850VA | 1000VA | 1.5kVA | -- | ADLS |
| 4 | 115VAC 1Ø | 12W | 15W | NA | -- | EDU |
| 5 | 28VDC | 80W | 100W | 120W (<50ms) | 50 | VCC |
| 6 | 28VDC | 80W | 100W | 120W | 10 | SMCC |
| 7 | 28VDC | 100W | 150W | 300W (<100ms) | 1ms @12A, then 20ms @1A | MCC |
| 8 | 28VDC | 900W | 1200W | 1300W | 10 | MIU |
| 9 | 28VDC | 100W | 200W | 500W (<100ms) | 0 | Roll/FMC  Motors |
| 10 | 28VDC | 200W | 300W | 350W (<100ms) | 10 | INS/EDU/  SPARE |

**TABLE II – System components and controllers**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Name | PCB | Output | Description | Controllers |
| SBC | SBC | N/A | System controller | FPGA |
| PFC | Main | Internal | Converts 3-phase 115VAC to 440VDC bus providing aux power to system and power to HV Buck | PFC micro |
| HV\_Buck | Main | Internal | Converts 440VDC to 85VDC bus providing power to several DCDCs | Buck micro |
| 3-phase relay | Filter | 3 | 3-phase 115VAC pass-through | N/A |
| 1-phase relay | Filter | 4 | 1-phase 115VAC pass-through | N/A |
| 50W DCDC | 50W DCDC | 2 | Converts 85VDC to 30.5V Output 2 | Primary-side secondary-side |
| DCDC1 | DCDC | 1 | Converts 28VDC to 36VDC | Primary-side secondary-side |
| DCDC4 | DCDC | 4 | Converts 85VDC to 28VDC | Primary-side secondary-side |
| DCDC5 | DCDC | 5 | Converts 85VDC to 28VDC | Primary-side secondary-side |
| DCDC6 | DCDC | 6 | Converts 85VDC to 28VDC | Primary-side secondary-side |
| DCDC7 | DCDC | 7 | Converts 85VDC to 28VDC | Primary-side secondary-side |
| LLC | 1k2W LLC | 8 | Converts 85VDC to 28VDC | Primary-side secondary-side |
| DCDC9 | DCDC | 9 | Converts 85VDC to 28VDC | Primary-side secondary-side |
| DCDC10 | DCDC | 10 | Converts 85VDC to 28VDC | Primary-side secondary-side |

Notes on communication lines:

1. All secondary-side micro controllers and the Buck micro communicate with the FPGA through RS485.
2. All secondary-side micro controllers communicate with the primary-side micro controllers through UART as well as dedicated logic lines.
3. The buck micro communicates with the PFC micro through UART as well as dedicated logic lines.
4. The FPGA has dedicated EN (enable) lines to PFC, 50WDCDC, DCDC1, DCDC4, DCDC5, DCDC6, DCDC7, LLC, DCDC9, DCDC10 and dedicated PG (Power Good) lines from HV\_Buck, 50WDCDC, DCDC1, DCDC4, DCDC5, DCDC6, DCDC7, LLC, DCDC9, DCDC10
5. The FPGA has enable lines to 3-phase relay and 1-phase relay

## FPGA Measurements

The FPGA must acquire measurements, some of which come from A/D channels, some of which come from communication with other system components through RS485 communication, and some which require calculation. Table III summarizes details of those measurements.

**Table III**

|  |  |  |
| --- | --- | --- |
| Measurement | Source | Details |
| VDC\_IN | DCDC1 RS485 | DCDC1 primary micro measures VDC\_IN and reports to DCDC1 secondary micro. Secondary micro reports VDC\_IN to FPGA through RS485. |
| VAC\_IN\_PH\_A | A/D on SBC | SBC A/D U48 CH1 represents instantaneous VAC\_IN\_PH\_A. Must calculate RMS. |
| VAC\_IN\_PH\_B | A/D on SBC | SBC A/D U48 CH2 represents instantaneous VAC\_IN\_PH\_B. Must calculate RMS. |
| VAC\_IN\_PH\_C | A/D on SBC | SBC A/D U48 CH3 represents instantaneous VAC\_IN\_PH\_C. Must calculate RMS. |
| I\_DC\_IN | A/D on SBC | SBC A/D U54 CH0 represents I\_DC\_IN |
| I\_AC\_IN\_PH\_A | A/D on SBC | SBC A/D U54 CH1 represents instantaneous phase A input current. Must calculate RMS. |
| I\_AC\_IN\_PH\_B | A/D on SBC | SBC A/D U54 CH2 represents instantaneous phase B input current. Must calculate RMS. |
| I\_AC\_IN\_PH\_C | A/D on SBC | SBC A/D U54 CH3 represents instantaneous phase C input current. Must calculate RMS. |
| V\_OUT\_2 | 50WDCDC RS485 | 50WDCDC secondary micro measures V\_OUT\_2 and reports to FPGA through RS485. |
| V\_OUT\_3\_ph1 | A/D on SBC | SBC A/D U48 CH7 represents instantaneous V\_OUT\_3\_ph1. Must calculate RMS. |
| V\_OUT\_3\_ph2 | A/D on SBC | SBC A/D U48 CH6 represents instantaneous V\_OUT\_3\_ph2. Must calculate RMS. |
| V\_OUT\_3\_ph3 | A/D on SBC | SBC A/D U48 CH5 represents instantaneous V\_OUT\_3\_ph3. Must calculate RMS. |
| V\_OUT\_4 | A/D on SBC | SBC A/D U48 CH0 represents instantaneous V\_OUT\_4. Must calculate RMS. |
| V\_OUT\_x  x = 1,5-7,9,10 | DCDCx RS485 | DCDCx secondary micro measures V\_OUT\_x and reports to FPGA through RS485. |
| V\_OUT\_8 | LLC RS485 | LLC secondary micro measures output voltage and reports to FPGA through RS485. |
| I\_OUT\_2 | 50WDCDC RS485 | 50WDCDC secondary micro measures I\_OUT\_2 and reports to FPGA through RS485. |
| I\_OUT\_3\_ph1 | Calculation | See note 1. Subtract instantaneous current I\_OUT\_4 and I\_PFC\_PH\_A from I\_AC\_IN\_PH\_A and calculate rms value. |
| I\_OUT\_3\_ph2 | Calculation | See note 1. Subtract instantaneous current I\_PFC\_PH\_B from I\_AC\_IN\_PH\_B and calculate rms value. |
| I\_OUT\_3\_ph3 | Calculation | See note 1. Subtract instantaneous current I\_PFC\_PH\_C from I\_AC\_IN\_PH\_C and calculate rms value. |
| I\_OUT\_4 | A/D on SBC | SBC A/D U48 CH4 represents instantaneous current through Output 4. Must calculate RMS. |
| I\_OUT\_x  x = 1,5-7,9,10 | DCDCx RS485 | DCDCx secondary micro measures I\_OUT\_x and reports to FPGA through RS485. |
| I\_OUT\_8 | LLC RS485 | LLC secondary micro measures I\_OUT\_x and reports to FPGA through RS485. |
| AC\_Power | Calculation | Running average of VAC\_IN\_PH\_A\* I\_AC\_IN\_PH\_A + VAC\_IN\_PH\_B\* I\_AC\_IN\_PH\_B + VAC\_IN\_PH\_C\* I\_AC\_IN\_PH\_C |
| Fan\_Speed\_1 | Hall sensor from Fan1 | Frequency of hall sensor3 same as fan speed. Change Hz to RPM. |
| Fan\_Speed\_2 | Hall sensor from Fan2 | Frequency of hall sensor2 same as fan2 speed. Change Hz to RPM. |
| Fan\_Speed\_3 | Hall sensor from Fan3 | Frequency of hall sensor3 same as fan3 speed. Change Hz to RPM. |
| T\_x  x = 1,5-7,9,10 | DCDCx RS485 | Temperature of DCDCx reported from DCDCx secondary through RS485. See note 2. |
| T\_2 | 50WDCDC RS485 | Temperature of 50WDCDC reported from 50WDCDC secondary through RS485. See note 2. |
| T\_8 | LLC RS485 | Temperature of LLC reported from LLC secondary through RS485. See note 2 |
| T\_main | HV\_BUCK RS485 | Temperature of Main Board reported from Buck through RS485. See note 2 |
| DC\_IN\_Status | Calculation | If 28VDC from Aircraft is within correct range, then logical 1; otherwise logical 0. See note 3. |
| AC\_IN\_Status | Calculation | If RMS values of VAC\_IN\_PH\_A, B, and C are in correct range, then logical 1; otherwise, logical 0. See note 4. |
| Power\_Out\_Status | Calculation | If all modules produce PG=1, then 1, otherwise 0. |
| OUTx\_OC  x = 1,5-7,9,10 | DCDCx RS485 | If PG goes low on any power supply unit, then the secondary of that unit must send status information to the FPGA via RS485 indicating if the shutdown occurred due to output overcurrent, output overvoltage, overtemperature, input voltage out-of-range, or another reason. |
| OUT2\_OC | DCDC2 RS485 |
| OUT8\_OC | LLC RS485 |
| DC\_IN\_OV | DCDC1 RS485 |
| OUTx OV  x = 1,5-7,9,10 | DCDCx RS485 |
| OUT2 OV | DCDC2 RS485 |
| OUT8 OV | LLC RS485 |
| DC\_IN\_UV | DCDC1 RS485 |
| AC\_IN\_UV | Calculation | See note 4. |
| PHx\_Status  x = 1, 2, 3 | Calculation | See note 4. Report according to voltage on each phase. |
| Neutral\_Status | Calculation | Normally a logical 1. Average of instantaneous sum of VAC\_IN\_PH\_A, VAC\_IN\_PH\_B, and VAC\_IN\_PH\_C should always be close to 0. If departing more than some threshold amount from 0, that indicates that the neutral fuse opened in which case the logical status will change to 0. |
| OVER\_TEMP\_Status | RS485 all PSUs | Logical 1 unless a PSU reports an overtemperature through the RS485 bus. |
| Capacitor\_end\_of\_life | Buck RS485 | See note 5. |
|  |  |  |

Note 1: Buck secondary reports rms PH1, PH2, and PH3 currents into PFC. FPGA estimates instantaneous current into PFC by assuming that the current is proportional to VAC\_IN\_PH\_A, VAC\_IN\_PH\_B, and VAC\_IN\_PH\_C but has the rms value reported from the buck secondary on the RS485. The FPGA can use this information to calculate instantaneous values of I\_PFC\_PH\_A, I\_PFC\_PH\_B, and I\_PFC\_PH\_C.

Note 2: The secondary of each micro can be configured to report temperature either as a 12-bit A/D value or each micro can calculate temperature according to NTC curve and report as an 8-bit integer representing temperature with a known offset.

Note 3: The 28VDC from the aircraft must remain within 18-32VDC for continuous operation; however, the input voltage is allowed to go outside these limits for short duration. Spec 3.2.10.3 Below 18V there is an immediate shutdown. The PSU must work at least according to MIL-STD 704A transients. Above 90V, DCDC1 will immediately shutdown without any warning time. For 80V – 90V, an emergency shutdown will be initiated. For 32V – 80V, the PSU can work for 5s and will then shut down. We must decide how much of this functionality is determined by the FPGA and how much by DCDC1.

Note 4: Spec 3.2.1.2 and 3.2.10.3 Between 95VAC and 125VAC the input AC voltage is OK. Between 90VAC and 95VAC, the input voltage is OK for 500ms and then a shut down must be initiated. Below 90VAC, there is an immediate shutdown. Above 125VAC, the PSU only needs to work according to MIL-STD 704A, but may work longer. MIL-STD 704A allows transients up to 180VAC for 150ms decreasing to 125VAC over the next 3s. If the input voltage goes above 180VAC, the PSU shuts down immediately. We must decide how much of these functions are done within the FPGA and how much is done by the PFC micro.

Note 5: Based on agreement during PDR, this requirement was removed. However, during development we can attempt to make this calculation and decide later whether it is accurate enough to use in production. HV\_BUCK bus capacitance value can be calculated when the PSU is shut down. Based on Buck load current and rate of fall of the bus, it is possible to calculate the bus capacitor value. When the capacitor value drops below a predetermined value, it can be assumed to be at end-of-life. This would need to be calculated and reported to the FPGA during the shutdown, and the FPGA needs to store this information. Once the PSU is turned back on, the capacitor end-of-life indication can be set high. Note that to reset the end-of-life indication would require cycling the PSU.

## Built-inTests (BIT)

After startup, the FPGA must request a built-in test (BIT) from each PSU module at an interval of 100Hz. Each PSU module then responds with the information it is required to provide the FPGA to satisfy the customer specification requirements for a BIT. See IRS document section 5 for details.  
  
If EN for the PSU module is low at the time the BIT is received, then the BIT is assumed to be a PUBIT (power up built-in test); otherwise, the BIT is assumed to be a periodic BIT. In the case of a PUBIT, the module will not push power, but only provide whatever information is possible given that the PSU is not powered up. The Main Board (PFC and HV\_BUCK) should be given an EN signal prior to the PUBIT since the main board can and should be powered completely during the PUBIT.  
Each PSU Module should provide a status byte with the BIT output. The status byte should include bits representing status of parameters appropriate for each PSU module, for example, output OVP, output OCP, output UV, internal OCP limits, internal OTP, internal DC bus OVP, internal DC bus UV, etc. The format of the status byte is TBD.

Writing to Flash  
The FPGA has an A/D reading of the 12V\_Redundant supply that creates all of the aux power for the SBC Board. When this supply drops below 8V for more than 1ms (level and duration may be modified according to testing), then the FPGA should immediately stop writing to the eMMC to prevent the possibility of trying to write to the eMMC while the power is going down. This test should be done frequently enough that there is no possibility for the SBC power to go down in the middle of a write operation to the eMMC (e.g. every 10ms).  
Note that when the JTAG is programming the eMMC, the 12V\_Redundant supply may be as low as 5V.

Startup Sequence

The PFC is connected to the 115VAC regardless of whether the PSU has been started or not. When the 115VAC is connected, the PFC micro will turn on the inrush protection FET based on bus capacitor charge and time, regardless of whether the PSU is running.

When a startup signal is received by the FPGA, the FPGA should turn on the fans and set EN high to the PFC micro. When PG is received from the Buck micro, the FPGA should set EN high to all of the other modules, to the three-phase relay (Output 3), and to the single-phase relay (Output 4).

Shutdown Sequences  
E-Shutdown

In the case of an emergency shutdown, after the E-shutdown discrete signal is set high, the FPGA must shut down PSU modules (setting EN low) according to required holdup times indicated in Table I. DCDC9 as well as the three-phase and single-phase relays shut down immediately. The 50WDCDC, the LLC, DCDC6, and DCDC10 shut down after 10ms. DCDC7 shuts down after 20ms. DCDC5 shuts down after 50ms. The fans should be turned off after a cool-down period TBD (Or we can decide to turn off the fans based on temperatures measured inside the PSU).  
  
Standard shutdown

In case of an overtemperature condition, the FPGA should set the discrete shutdown high and then disable all power supplies after 10s (3.1.5.2, 3.2.10.5). CCTCU and ECTCU should be set low after disabling the internal power supplies. The fans should be turned off after a cool-down period TBD (Or we can decide to turn off the fans based on temperatures measured inside the PSU).

Reverse Voltage

A reverse voltage condition will not occur during normal operation – it would only occur when power is first applied from the aircraft. In case of a reverse voltage, the 28V from the aircraft will appear to be 0V. The fans will not run and DCDC1 will not be powered. Since DCDC1 will not be powered, it will have no communication with the FPGA. If DCDC1 has no communication with the FPGA and the fan speed is 0, then the FPGA should assume that the 28V from the aircraft is 0V (whether from not being present or a reverse voltage) and the PSU should not startup. The 28V from the aircraft will be reported as 0V.

## Input OVP

If the input AC voltage has an OVP condition (transient above 180VAC, 3.2.10.2.1), the PFC and HV\_Buck will immediately stop switching. The FPGA, which is also measuring the input AC voltage, should immediately shut down all power supplies and communication lines. If the OVP condition disappears continuously for 1s, the FPGA should restart the system.

If the aircraft 28V has an overvoltage, it will immediately shut down the primary side switching but continue to report the input voltage to the secondary-side micro. The secondary-side micro will report the overvoltage condition to the FPGA which will immediately turn off the fans and all PSUs. If the OVP condition disappears continuously for 1s, the FPGA should restart the system.

## Output OVP

Based on 3.2.10.2.2 If any output voltage exceeds the corresponding over-voltage trip point threshold for more than the rated duration, the PSU shall immediately disable the faulty output and send an emergency shutdown discrete to the MIU, and then turn off all remaining outputs after corresponding hold-up time.

After the over-voltage protection has been activated, the PSU shall turn-on again only after the ON/OFF switch is driven low and then asserted high again after a minimum period of 1s (i.e. no automatic recovery after an output over-voltage fault event).

The rated output OVP table from the customer specification is as follows:

|  |  |  |
| --- | --- | --- |
| **Voltage** | **O.V. Trip Point** | **Detection Response Time** |
| 115VAC | 125VAC | 100msec |
| 28VDC | 35VDC | 2ms |
| 30.5VDC | 31.5% | 2ms |
| 36VDC | 45 VDC | 2ms |

## Notes on Relays (Outputs 3 and 4)

Output 3 is a mechanical relay. Timing of the coil is not critical. The rms outputs from each phase should be similar to the three phase rms inputs. If the rms outputs differ from the rms inputs by more than TBD percentage (let’s say 3%), then that is equivalent to Output 3 PG being low. However, due to the time it takes the relay contact to close and the time required to compute rms voltages, the rms input and output measurements should not be compared until the output measurement has stabilized.

Output 4 is a semiconductor switch. Turn on needs to occur near the zero-crossing of phase A to reduce inrush current. Therefore when the command to turn on Output 4 is received, the FPGA should not turn on the single-phase relay until the voltage across Phase A is close to zero – let’s say between -5V and +5V. As with Output 3, determination of PG for Output 4 also depends on comparison of Phase A input rms to Output 4 rms, except that the voltage drop for Output 4 is higher than for Output 3. Allow the rms voltages between input and output to differ by 10% before causing PG for Output 4 to be low.

## Note on Lamp Status

The lamp\_status\_fpga is a logic signal checking whether the cockpit lamp is receiving voltage. lamp\_status\_fpga should be the same logic as pod\_status\_fpga (with a short delay < 10us) if the circuit driving the cockpit lamp is working. If the logic is different, aside from the short turn-on and turn-off delay, then the lamp circuit is not working. There is currently no requirement to report this; however, the customer IRS document includes non-assigned spare status bytes, so this information might be reported in the future.

## Note on Hall Sensors

Several of the hall sensors include a zero-current reference (e.g. ZCR\_sns\_ADC\_CS\_fpga). The purpose of this measurement is to determine the voltage out of an AC hall sensor which represents zero current. The zero-current reference voltage should be subtracted from the current measurement output voltage to determine the actual ac current which is being measured.